**Lab Assignment 1 (20 Marks)**

**Show the output to instructor on 30/9/2020**

**Exercise.1:** Design and implement a **Moore-**based FSM for a conference room light automation system. The FSM has two inputs (other than Reset (T18) and Clock (Y9) which are not shown in figure): Ambient light indicator (A) and person detector (P); and one output O.

A (F22)

O (T22)

P (G22)

FSM

The Ambient light sensor indicator A is logic ‘1’ when there is enough natural light in the room, else it is logic ‘0’. The person detector P gives logic ‘1’ if there is any one present in the room and logic ‘0’ if there is nobody in the room.

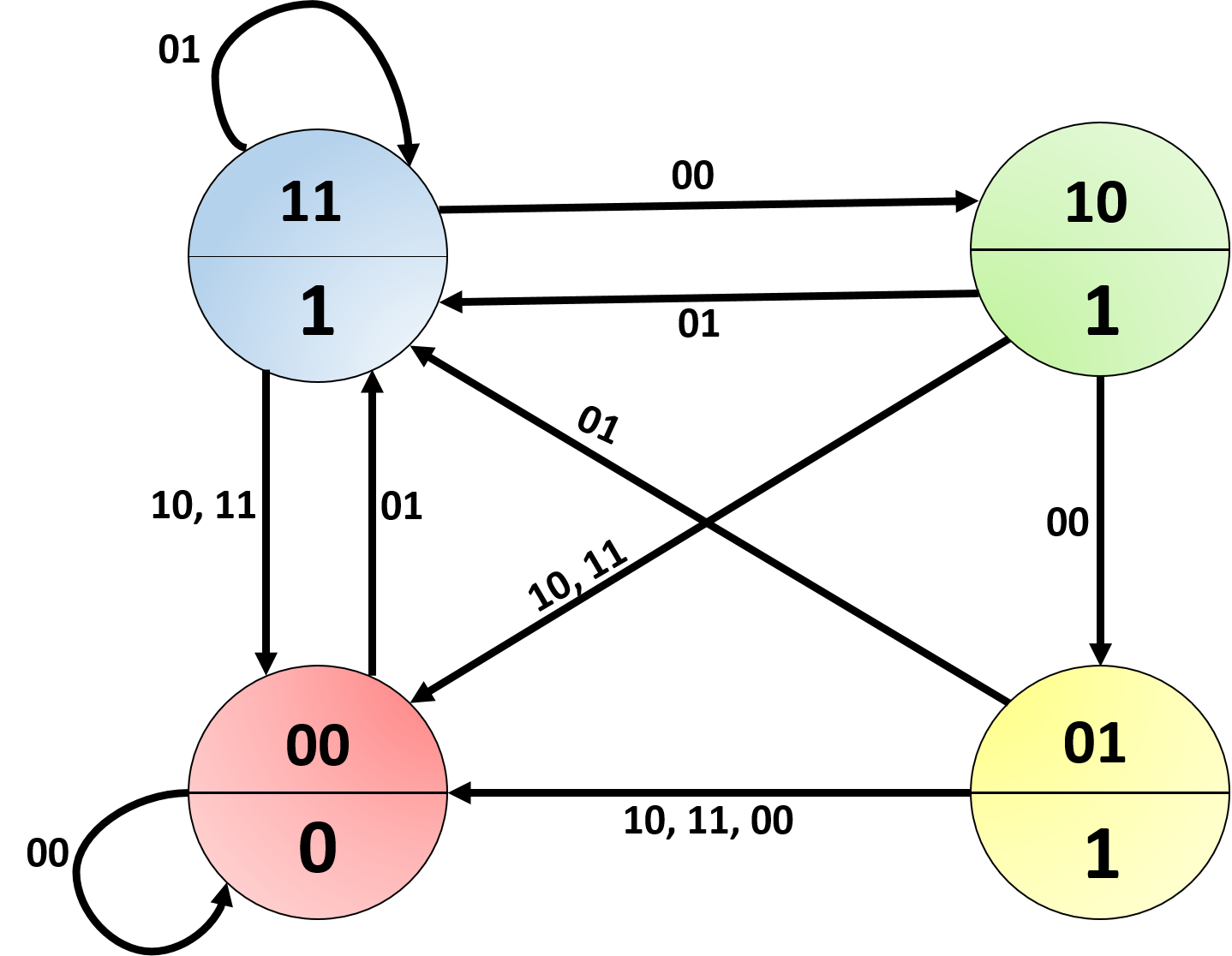
The system has an output (O) which is connected to the light. O=logic ‘1’ indicates light is ON and O=logic ‘0’ indicates light is OFF. The output O is controlled as below:

If the light is OFF, it will switch ON only when there is not enough natural light and at least one person is present in the room.

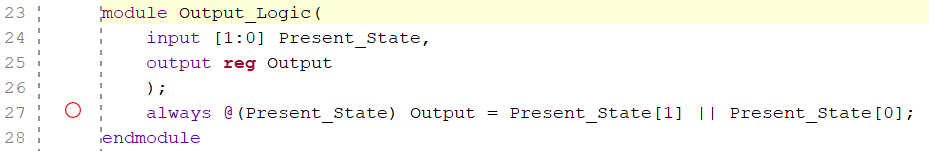
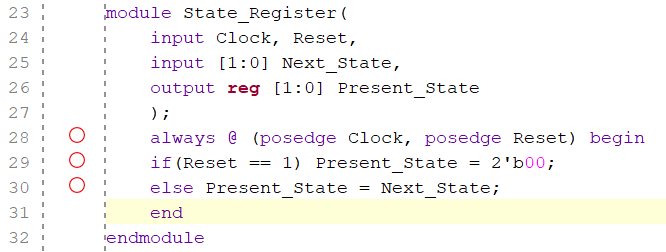
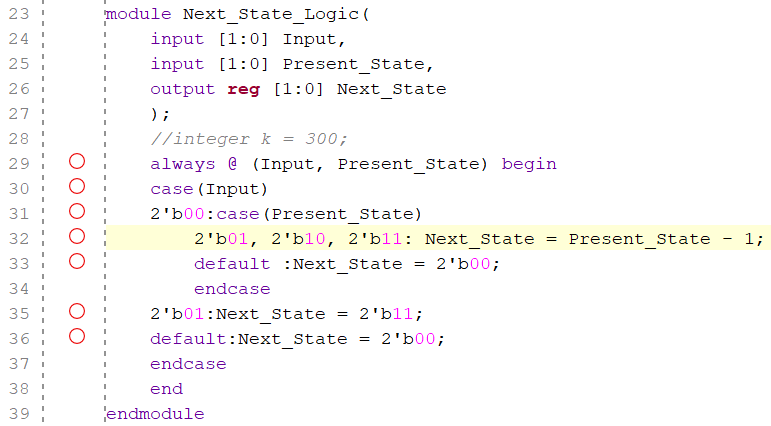
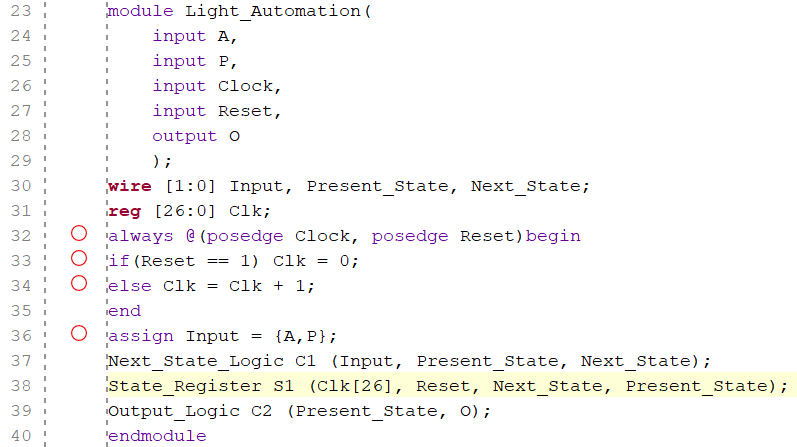
If the light is ON, it should switch OFF as soon as there is enough natural light.

If the light is ON and if there is not enough natural light, then the light should switch OFF only if nobody is in the room for more than 3 sec, i.e. once the room becomes empty, the light should switch OFF after 3 Seconds. If somebody walks into the room within the 3 sec time limit the light remains ON. If there is enough light within 3 sec time limit, the light switches OFF (Hint: If FSM uses a Clock of 1Hz then 3 Sec is equivalent to 3 clock cycles). When reset is enabled the FSM will be in a state where light is OFF. Any other assumptions should be clearly mentioned below.

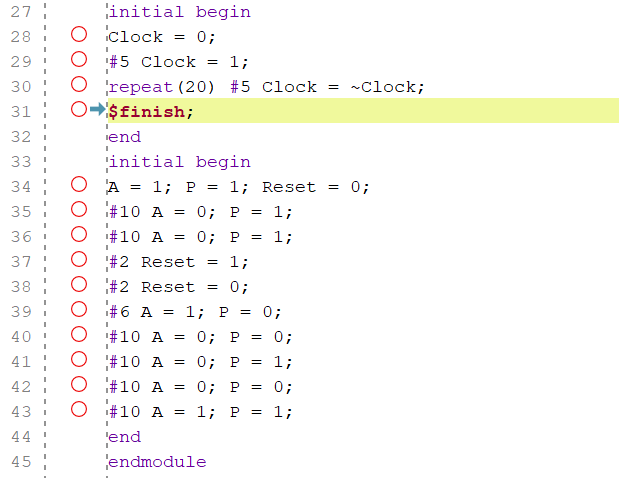
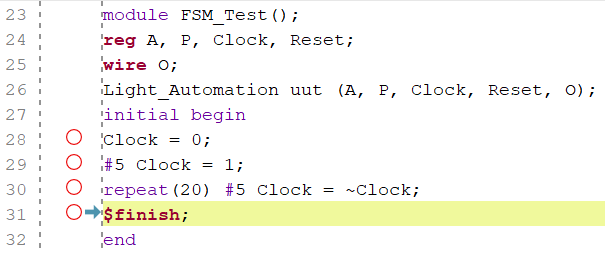
1. **Copy the image of FSM for the above specification (Clearly label all inputs and outputs).**

Answer:

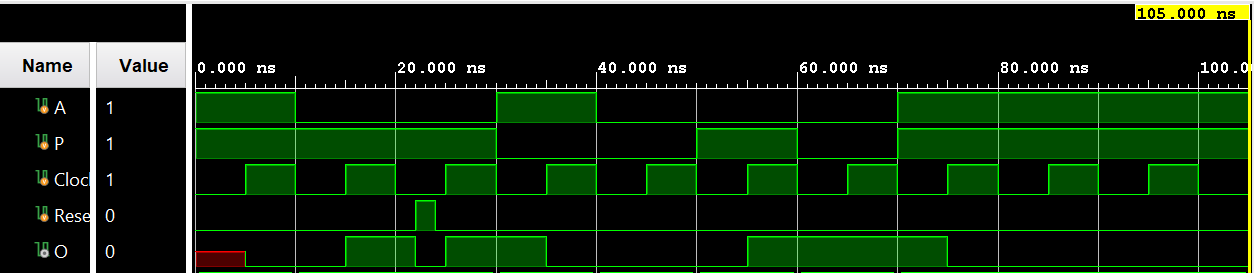
1. **Copy the image of all your Verilog (main and sub modules) Codes below.**

Answer: 1 main module + 3 sub-modules (Next State Logic, State Register, Output Logic) 

1. **Copy the image of Test Bench Verilog code below.**

Answer:

1. **Copy behavioral simulation waveform (without clock division) window below.**

Answer:

1. **Implement the design on FPGA after including clock division (Elaborate, I/O Plan, Synthesize, Implement, Bitstream and Program) and verify the outputs.**
2. **Check the output on FPGA.**
3. **Show the output to the instructor.**
4. **Submit following files as a Zipped folder with file name as <Student\_ID\_No>.zip through Google classroom before due date.**

**1) Completed Document**

**2) All source files (design, Test Bench and Constraints)**

**3) Bitstream file**

**4) Txt file showing pin assignment else you can use the pin assignment shown in Figure above**